REMARKS

Claims 1-20 stand rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the speification in such a way as to enable one skilled in the art to make and/or use the invention. Claims 1, 3, 6 and 8 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S Patent No. 6,306,706, to Chan et al (hereinafter "Chan"). Claims 4, 7 and 9 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chan in view of U.S. Patent No. 5,284,549 to Barnes et al. (hereinafter "Barnes"). Claims 9 and 18 have been amened to clarify the claimed invention. Claims 1- 20 are in the application. Claims 1 and 10 are independent.

The specification has been amended to correct a typographical error. Title has been amened to better described the claimed invention.

Regarding the Examiner's comment of claims 10-20, "Claims 10-20 pertain to a device while the Application pertain to a method hence they do not have patentable weight," Applicants respectffuly submit claims 10-17 and 19-20 are proper Product-by-Process claims, see MPEP 706.03(e), which states: "An article may be claimed by a process of making it..." If the Examiner objects to these claims, Applicants request clairifation of such an objection and to the above comment of the present Office Action.

On the merits, Applicant respectfully submits that the pending claims, as amended, are patentable for at least the following reasons.

Claims 1-20 stand rejected under 35 U.S.C. 112, first paragraph. In particular, claim 1 recites the limitation of partially depositing an etch stop layer. This limitation is fully supported in the specificaiotn at least on page 5, line 9 through page 6, line 13 and

FIG. 1B. Moreover, Applicants agree with the Examiner's charicterzation that the etch stop layer is selectively deposited on an etching area of a first silica layer, as shown in FIG. 1B. Nevertheless, Applcants have amended claim 1 to more particulary point out the invention.

Claim 2 recites: wherein the etch stop layer deposition step comprises the steps of depositing a photoresist layer on the first silica layer; patterning the photoresist layer according to the shape of the etching area; forming the etch stop layer on the surfaces of the photoresist layer and the first silica layer; and removing the photoresist layer using a photoresist remover. These limitations are fully supported in the specification at least on page 6, line 14 through page 7, line 16. Appliicant respecfully note in response the Examiner's question, that the photoresist layer is patterned, thus can be removed without removing the etch stop layer. Nevertheless, Applcants have amended claim 2 to more particulary point out the invention.

Accordingly, Applicants believe claims 1-20 are patentable under 35 U.S.C. 112.

Amended independent claim 1 is directed a silica microstructure fabrication method comprising the steps of depositing an etch stop layer on an etching area of a portion of a first silica layer formed on a semiconductor substrate, forming a second silica layer on the surfaces of the etch stop layer and the first silica layer, forming a mask patterned according to the shape of the etching area on the surface of the second silica layer, removing the second silica layer from the etching area using the mask by dry etching; and removing the etch stop layer by wet etching. Amended independent claim 10 recites similar limitations.

Chan, as read by the applicants, relates to a method for fabricating a flash memory array comprising a core area and a periphery area. The method comprises depositing a layer of poly2 over the core area and the periphery area, selectively etching the core area, and selectively etching the poly2 only in the periphery area wherein the occurrence of stringers is reduced. The core and periphery areas are etched separately after the deposition of the poly2, thereby reducing the occurrence of stringers at the core/periphery interface.

Chan fails to teach, show or suggest depositing an etch stop layer on an etching area of a portion of a first silica layer formed on a semiconductor substrate, forming a second silica layer on the surfaces of the etch stop layer and the first silica layer, forming a mask patterned according to the shape of the etching area on the surface of the second silica layer, removing the second silica layer from the etching area using the mask by dry etching; and removing the etch stop layer by wet etching, as specifically recited in amended claim 1.

The Office Action indicates Chan, in figure 5, teaches the claimed limitiations. Applicants respectfully disagree. In this regard, applicants have found no indication in Chan that even shows any recognition of the advantages or the desirability of the limitations recited in claim 1. For example, Jackson, in figure 5, shows that the core and periphery regions of a flash memory are etched separately after the deposition of poly2 layer, thereby reducing the occurrence of stringers at the core/periphery interface. The poly layers in Chan (poly1 and poly2) are polysilicon, which are used to form transistors and connections therebetween, see col. 1 lines15-20 and lines 45-60 of Chan. Moreover, Applicants can find nothing in Chan that teaches an entch stop layer having a high etch

selectivity with respect to silica, such as gold and platinum, see specification on page 6, lines 6-12.

It is well settled that a reference that does not teach or suggest all of the features of a claimed invention cannot anticipate that invention. Since Chan does not teach or suggest all of the features of amended independent claims 1 and 10, as recited above, applicant respectfully submits that these claims are allowable and patentable under 35 U.S.C. § 102.

Claims 2-20 in this application are each dependent from one or the other of independent claims discussed above and are, therefore, believed allowable and patentable under 35 U.S.C. § 102 and 103 for the same reasons.

A review of the other art of record has failed to reveal anything which, in the applicants' opinion, would remedy the deficiencies of the art discussed above as referenced against the claims now present in this application. The claims are, therefore, believed patentable over the art of record.

In view of the foregoing remarks, applicants respectfully request favorable reconsideration and early passage to issue of the present application.

Should the Examiner deem that there are any issues which may be best resolved by telephone, please contact Applicant's undersigned representative at the number listed below.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Patent Application of

Inventor(s): Dong-Su Kim Group Art Unit: 2823

Serial No.: 09/899,784 Examiner: Toledo, Fernando L

Filing Date: July 5, 2001

For: Method of Fabricating Silica Microstructures

Assistant Commissioner for Patents
Washington, D.C. 20231

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE

Please replace the title as follows:

-- "SILICA MICROSTRUCTURE AND FABRICATION METHOD THEREOF" --

IN THE SPECIFICATION

Please amend the specification as follows:

Page 5, in the paragraph beginning on line 12, change as follows:

FIG. 1B illustrates the step of partially depositing an etch stop layer ~~1~~13 on an etching area of the first silica layer 12. The etch stop layer 13 is partially deposited by loft-off or etching.